CLIPPEDIMAGE= JP404134827A
PAT-NO: JP404134827A
DOCUMENT-IDENTIFIER: JP 04134827 A
TITLE: MANUFACTURE OF SEMICONDUCTOR DEVICE
PUBN-DATE: May 8, 1992
INVENTOR-INFORMATION:
NAME
ONO, TOSHIKO
ASSIGNEE-INFORMATION:

NAME	COUNTRY
TOSHIBA CORP	N/A

APPL-NO: JP02255124
APPL-DATE: September 27, 1990
INT-CL (IPC): H01L021/3205
US-CL-CURRENT: 438/FOR.395,438/FOR.492 ,438/763 ,438/978

ABSTRACT:
PURPOSE: To improve reliability and reduce wiring capacitance by preventing any cavity from being produced by forming a reverse tapered groove in an interlayer insulating film on a semiconductor substrate correspondingly to a wiring pattern and burying the groove with a wiring material.

CONSTITUTION: A groove corresponding to a wiring pattern is formed in an interlayer insulating film 2 deposited on a semiconductor substrate 1 with a wiring shape thereof being reversely tapered. Thereafter, wiring is formed by burying the groove with a single or a plurality of layers of a wiring material 3. With the resulting reverse taper-shape, burying of the wiring material into the groove is facilitated to restrict cavity production for improvement of reliability and reduction of wiring capacitance. Further, flattening of the top layer is facilitated.

DERWENT-ACC-NO: 1992-204646
DERWENT-WEEK: 199225

TITLE: Semiconductor device mfr. - includes digging reverse taper corresp.
wiring pattern and burying wiring material in it to be planar NoAbstract

PATENT-ASSIGNEE: TOSHIBA KK[TOKE]

PRIORITY-DATA: 1990JP-0255124 (September 27, 1990)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 04134827 A	May 8, 1992	N/A	007	H01L 021/3205

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
JP04134827A	N/A	1990JP-0255124	September 27, 1990

INT-CL (IPC): H01L021/3205; H01L021/88
ABSTRACTED-PUB-NO:
EQUIVALENT-ABSTRACTS:

TITLE-TERMS:
SEMICONDUCTOR DEVICE MANUFACTURE DIG REVERSE TAPER CORRESPOND WIRE PATTERN BURY
WIRE MATERIAL PLANE NOABSTRACT

DERWENT-CLASS: L03 U11

CPI-CODES: L04-C10A;

EPI-CODES: U11-C05D3;

SECONDARY-ACC-NO:
CPI Secondary Accession Numbers: C1992-093072
Non-CPI Secondary Accession Numbers: N1992-154825

CLIPPEDIMAGE= JP411330075A
PAT-NO: JP411330075A
DOCUMENT-IDENTIFIER: JP 11330075 A
TITLE: SEMICONDUCTOR DEVICE
PUBN-DATE: November 30, 1999
INVENTOR-INFORMATION:

NAME	COUNTRY
AKAHORI, TAKASHI	N/A

ASSIGNEE-INFORMATION:

NAME	COUNTRY
TOKYO ELECTRON LTD	N/A

APPL-NO: JP10140584
APPL-DATE: May 7, 1998
INT-CL_(IPC): H01L021/3205; H01L021/314
ABSTRACT:
PROBLEM TO BE SOLVED: To suppress the diffusion of Cu to an insulating film,
when Cu is used as a wiring material.

SOLUTION: An insulating film is formed of CF films 21-24. Cu wiring layers 25
and 26 are formed on the CF films 21-24 via adhesion layers 29 formed of a Ti
layer and a TiC layer. Since Cu does not diffuse into the CF films 21-24, the
damages of an element owing to the diffusion of Cu to the CF films 21-24 is
suppressed, and the quality of a semiconductor device can be improved.

CLIPPEDIMAGE= JP411186274A
PAT-NO: JP411186274A
DOCUMENT-IDENTIFIER: JP 11186274 A
TITLE: DUAL DAMASCENE TECHNIQUE
PUBN-DATE: July 9, 1999
INVENTOR-INFORMATION:

NAME	COUNTRY
YO, BUNKAN	N/A
RIN, KENTEI	N/A
CHIN, SHINRAI	N/A
KO, KOSEI	N/A

ASSIGNEE-INFORMATION:

NAME	COUNTRY
UNITED MICROELECTRON CORP	N/A
UNITED MICROELECTRON CORP	N/A

APPL-NO: JP10135315
APPL-DATE: May 18, 1998
INT-CL (IPC): H01L021/3205; H01L021/768
ABSTRACT:
PROBLEM TO BE SOLVED: To provide a dual damascene technique which is capable of preventing etching damages and making a change small in critical dimensions.

SOLUTION: A first and a second photoresist layer are each previously formed in the prescribed regions of a narrow opening and a wide opening of a dual damascene. A composite layer 37 composed of an HSQ(hydrogen silsesquioxane) layer 34 and an oxide layer 36 provided on the layer 34 is formed surrounding the first and second photoresist layer respectively. After the photoresist layers are removed, the left opening 42 is filled up with an adhesive/barrier layer and a metal layer 40.

DERWENT-ACC-NO: 1999-450100
DERWENT-WEEK: 200027

TITLE: Dual damask technique used in integrated circuit IC manufacture -
involves removing first photoresist layer and second photoresist layer in order
to form opening, and filling opening with metal

INVENTOR: LIU, M; LUR, W ; SUN, S ; YEW, T

PATENT-ASSIGNEE: LIANHUA ELECTRONICS CO LTD[LIANN], UNITED MICROELECTRONICS
CORP[UNMIN]

PRIORITY-DATA: 1997TW-0119307 (December 19, 1997)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
TW 360949 A	June 11, 1999	N/A	000	H01L 021/768
JP 11186274 A	July 9, 1999	N/A	006	H01L 021/3205

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
TW 360949A	N/A	1997TW-0119307	December 19, 1997
JP 11186274A	N/A	1998JP-0135315	May 18, 1998

INT-CL_(IPC): H01L021/3205; H01L021/768

ABSTRACTED-PUB-NO: JP 11186274A
BASIC-ABSTRACT: NOVELTY - A silicon oxide layer (36), which has a uniform
surface, is formed such that its height is equal to the height of a second
photoresist layer. A first photoresist layer and the second photoresist layer
are removed in order to form an opening (42). The opening is filled with a

metal (40).

USE - Used in IC manufacture.

ADVANTAGE - Prevents damage caused by etching, and minimizes variation of limit size. DESCRIPTION OF DRAWING(S) - The figure shows the explanatory sectional view of a dual damask technique. (36) Silicon oxide layer; (40) Metal; (42) Opening.

CHOSEN-DRAWING: Dwg.3/10

TITLE-TERMS:
DUAL TECHNIQUE INTEGRATE CIRCUIT IC MANUFACTURE REMOVE FIRST PHOTORESIST LAYER
SECOND PHOTORESIST LAYER ORDER FORM OPEN FILL OPEN METAL

DERWENT-CLASS: U11

EPI-CODES: U11-C04A1C; U11-C04D; U11-C05D;

SECONDARY-ACC-NO:
Non-CPI Secondary Accession Numbers: N1999-336581

CLIPPEDIMAGE= JP411186261A
PAT-NO: JP411186261A
DOCUMENT-IDENTIFIER: JP 11186261 A
TITLE: MANUFACTURE OF SEMICONDUCTOR DEVICE
PUBN-DATE: July 9, 1999
INVENTOR-INFORMATION:

NAME	COUNTRY
TAKAGI, HIDEO	N/A
UJI, SHIGETAKA	N/A
ENDO, KOJI	N/A
MISAWA, NOBUHIRO	N/A
MIZUSHIMA, MASAKO	N/A
MURAKAMI, SATOSHI	N/A
ANTHONY, HOBBES	N/A

ASSIGNEE-INFORMATION:

NAME	COUNTRY
FUJITSU LTD	N/A

APPL-NO: JP09350393
APPL-DATE: December 19, 1997
INT-CL (IPC): H01L021/3205
ABSTRACT:
PROBLEM TO BE SOLVED: To enhance a wiring layer structure in reliability in the manufacture of a semiconductor device, by a method wherein voids are prevented from being generated in a Cu buried wiring layer or a Cu plug, and the Cu buried wiring layer or the Cu plug is enhanced in grain size so as to improve resistance to electromigration.

SOLUTION: A recess 3 is provided to an insulating layer 2 formed on a board 1 so as to provide a wiring layer or a plug into it, a Cu layer 5 is filled in the recess 3 through the intermediary of a base conductive film 4, a disused part of the Cu layer 5 is removed through a chemical mechanical polishing

method for the formation of a Cu buried layer 6, and then impurities are
removed from the Cu buried layer 6 through a thermal treatment.

DERWENT-ACC-NO: 1999-450089
DERWENT-WEEK: 199938

TITLE: Copper@ embedded layer impurity desorption process in semiconductor manufacture - involves removal of unnecessary copper@ forming copper embedding layer and heat-treating to remove impurity

PATENT-ASSIGNEE: FUJITSU LTD[FUIT]

PRIORITY-DATA: 1997JP-0350393 (December 19, 1997)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 11186261 A	July 9, 1999	N/A	017	H01L 021/3205

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
JP11186261A	N/A	1997JP-0350393	December 19, 1997

INT-CL_(IPC): H01L021/3205

ABSTRACTED-PUB-NO: JP11186261A

BASIC-ABSTRACT: NOVELTY - Copper (5) is filled into a recess (3) on an insulating layer through an electrically conductive film (4). A copper embedding layer (6) is formed by removing unnecessary copper layer by chemo-mechanic al polish method. The copper embedding layer is heat treated to make the impurity desorb.

USE - For removing impurity from copper imbedding layer in semiconductor device.

ADVANTAGE - Improves electromigration resistance and reliability of high speed

integration semiconductor device, since grain size of copper wiring and copper
plug is enlarged.

DESCRIPTION OF DRAWING - The figure is an explanatory drawing of wiring layer
structure for impurity desorption in semiconductor device manufacturing method.
(3) Recess; (4) Conductive film; (5) Copper; (6) Copper embedding layer.

CHOSEN-DRAWING: Dwg.1/14

TITLE-TERMS:
COPPER@ EMBED LAYER IMPURE DESORB PROCESS SEMICONDUCTOR MANUFACTURE REMOVE
UNNECESSARY COPPER@ FORMING COPPER EMBED LAYER HEAT TREAT REMOVE IMPURE

DERWENT-CLASS: L03 U11

CPI-CODES: L04-C10D;

EPI-CODES: U11-C05C9;

SECONDARY-ACC-NO:
CPI Secondary Accession Numbers: C1999-132377
Non-CPI Secondary Accession Numbers: N1999-336570

CLIPPEDIMAGE= JP411191676A
PAT-NO: JP411191676A
DOCUMENT-IDENTIFIER: JP 11191676 A
TITLE: INTERCONNECTING STRUCTURE BY COPPER STUD WITH HEAT-RESISTANT METAL
LINER
PUBN-DATE: July 13, 1999
INVENTOR-INFORMATION:

NAME	COUNTRY
JAMES, M E HARPER	N/A
ROBERT, M JEFFKEN	N/A

ASSIGNEE-INFORMATION:

NAME	COUNTRY
INTERNATL BUSINESS MACH CORP <IBM>	N/A

APPL-NO: JP10272700
APPL-DATE: September 28, 1998
INT-CL_(IPC): H05K003/46; H01L021/768
ABSTRACT:
PROBLEM TO BE SOLVED: To provide a multilayered interconnecting electronic component which is prolonged in electromigration life.

SOLUTION: Interconnection is made into a stub form, and a vertical sidewall provided with a heat-resistant metal diffused barrier linear 15 which extends along it is included. A stub 14 has no barrier layer at the bottom, and the bottom of the stud 14 is brought into contact with a metal coating 12 on the dielectric layer 11 of a part. A continuos or discontinuous adhesive layer is provided between the bottom of the stud 14 and the surface of the metal coating 12. It is preferable that the adhesive layer be formed of a metal such as aluminum or the like which melts down in the stud 14 or the metal coating 12, when a part is heated during its formation or use. A suitable component employs a dual damask structure.

DERWENT-ACC-NO: 1999-386360
DERWENT-WEEK: 200210

TITLE: Interconnection structure of multilayered electronic component in semiconductor package, has liner which is configured along side wall of trench, which acts as diffusion barrier to dielectric layer

INVENTOR: GEFFKEN, R M; HARPER, J M E

PATENT-ASSIGNEE: INT BUSINESS MACHINES CORP[IBMC], IBM CORP[IBMC]

PRIORITY-DATA: 1997US-0941857 (September 30, 1997) , 2000US-0553581 (April 20, 2000)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
KR 279322 B	February 1, 2001	N/A	000	H01L 029/786
CN 1213851 A	April 14, 1999	N/A	001	H01L 021/768
SG 70654 A1	February 22, 2000	N/A	000	H01L 023/055
KR 99029770 A	April 26, 1999	N/A	000	H01L 029/786
US 6150723 A	November 21, 2000	N/A	000	H01L 023/485
TW 404034 A	September 1, 2000	N/A	000	H01L 023/522
JP 11191676 A	July 13, 1999	N/A	008	H05K 003/46
US 6300236 B1	October 9, 2001	N/A	000	H01L 021/4763

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
KR 279322B	N/A	1998KR-0037790	September 14, 1998
KR 279322B	Previous Publ.	KR 99029770	

	N/A	
CN 1213851A	N/A	1998CN-0119730
	September 29, 1998	
SG 70654A1	N/A	1998SG-0003808
	September 23, 1998	
KR 99029770A	N/A	1998KR-0037790
	September 14, 1998	
US 6150723A	N/A	1997US-0941857
	September 30, 1997	
TW 404034A	N/A	1998TW-0113991
	August 25, 1998	
JP 11191676A	N/A	1998JP-0272700
	September 28, 1998	
US 6300236B1	Div ex	1997US-0941857
	September 30, 1997	
US 6300236B1	N/A	2000US-0553581
	April 20, 2000	
US 6300236B1	Div ex	US 6150273
	N/A	

INT-CL_(IPC): H01L021/28; H01L021/31 ; H01L021/3205 ; H01L021/4763 ;
H01L021/768 ; H01L023/055 ; H01L023/485 ; H01L023/52 ; H01L023/522 ;
H01L023/525 ; H01L029/786 ; H05K003/46

ABSTRACTED-PUB-NO: CN 1213851A
BASIC-ABSTRACT: NOVELTY - A trench (14) is formed extending copper coating (12)
formed on dielectric layer (11). A metal diffusion barrier liner (15)
configured along side wall of the trench acts as diffusion barrier to the
dielectric layer. A copper layer filled in the trench is made to contact the
copper coating electrically.

DETAILED DESCRIPTION - The dielectric layer includes either silicon oxide,
fluorine oxide, polymer, diamond-like carbon film and span glass. A
discontinuous cementing layer is formed between two copper layers. The
cementing layer is not a diffusion barrier for copper. INDEPENDENT CLAIMS are
also included for the following:

(a) multilayered electronic component;

(b) multilayered electronic component manufacturing method

USE - For interconnecting multilayered electronic component in semiconductor package used in computer, telecommunication, military affairs, consumer application etc.

ADVANTAGE - Provides multilayered electronic component with improved electromigration durability.

DESCRIPTION OF DRAWING(S) - The figure shows the cross-sectional perspective diagram of tmultilayered electronic component.

Dielectric layer 11

Copper coating 12

Trench 14

Metal diffusion barrier liner 15

ABSTRACTED-PUB-NO: JP 11191676A
EQUIVALENT-ABSTRACTS: NOVELTY - A trench (14) is formed extending copper coating (12) formed on dielectric layer (11). A metal diffusion barrier liner (15) configured along side wall of the trench acts as diffusion barrier to the dielectric layer. A copper layer filled in the trench is made to contact the copper coating electrically.

DETAILED DESCRIPTION - The dielectric layer includes either silicon oxide, fluorine oxide, polymer, diamond-like carbon film and span glass. A discontinuous cementing layer is formed between two copper layers. The cementing layer is not a diffusion barrier for copper. INDEPENDENT CLAIMS are also included for the following:

(a) multilayered electronic component;

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ADVANTAGE - Provides multilayered electronic component with improved electromigration durability.

DESCRIPTION OF DRAWING(S) - The figure shows the cross-sectional perspective diagram of tmultilayered electronic component.

Dielectric layer 11

Copper coating 12

Trench 14

Metal diffusion barrier liner 15

US 6300236B

NOVELTY - A trench (14) is formed extending copper coating (12) formed on dielectric layer (11). A metal diffusion barrier liner (15) configured along side wall of the trench acts as diffusion barrier to the dielectric layer. A copper layer filled in the trench is made to contact the copper coating electrically.

DETAILED DESCRIPTION - The dielectric layer includes either silicon oxide, fluorine oxide, polymer, diamond-like carbon film and span glass. A discontinuous cementing layer is formed between two copper layers. The cementing layer is not a diffusion barrier for copper. INDEPENDENT CLAIMS are also included for the following:

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application etc.

ADVANTAGE - Provides multilayered electronic component with improved
electromigration durability.

DESCRIPTION OF DRAWING(S) - The figure shows the cross-sectional perspective
diagram of tmultilayered electronic component.

Dielectric layer 11

Copper coating 12

Trench 14

Metal diffusion barrier liner 15

CHOSEN-DRAWING: Dwg.1/8 Dwg.1/8

TITLE-TERMS:
INTERCONNECT STRUCTURE MULTILAYER ELECTRONIC COMPONENT SEMICONDUCTOR PACKAGE
LINING CONFIGURATION SIDE WALL TRENCH ACT DIFFUSION BARRIER DIELECTRIC LAYER

DERWENT-CLASS: U11 U14 V04

EPI-CODES: U11-C05D3; U11-D03B2; U14-H03B1; V04-R05A; V04-R07L; V04-R07P;

SECONDARY-ACC-NO:
Non-CPI Secondary Accession Numbers: N2001-108025

DERWENT-ACC-NO: 2000-023674
DERWENT-WEEK: 200168

TITLE: Non diffusing copper interconnect structure for semiconductor device

INVENTOR: AKAHORI, T

PATENT-ASSIGNEE: TOKYO ELECTRON LTD[TKEL]

PRIORITY-DATA: 1998JP-0140584 (May 7, 1998)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
KR 2001043347 A	May 25, 2001	N/A	000	H01L 021/768
	November 11, 1999	J	039	H01L 021/768
WO 9957760 A1	November 30, 1999	N/A	014	H01L 021/3205
JP 11330075 A	February 21, 2001	E	000	
EP 1077486 A1	September 1, 2000	N/A	000	H01L 021/768
TW 403942 A				H01L 021/205

DESIGNATED-STATES: IL KR SG US AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL P
T SE BE DE FR IT

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
KR2001043347A	N/A	2000KR-0712346	November 6, 2000
WO 9957760A1	N/A	1999WO-JP02363	May 6, 1999
JP 11330075A	N/A	1998JP-0140584	May 7, 1998
EP 1077486A1	N/A	1999EP-0918319	May 6, 1999
EP 1077486A1	N/A	1999WO-JP02363	

May 6, 1999
EP 1077486A1 Based on WO 9957760
N/A
TW 403942A N/A 1999TW-0107295
May 5, 1999

INT-CL (IPC): H01L021/205; H01L021/314 ; H01L021/3205 ; H01L021/768

ABSTRACTED-PUB-NO: WO 9957760A
BASIC-ABSTRACT: NOVELTY - Insulating films (21-24) constituted of CF films (fluorine-containing carbon films) are formed on a substrate. Cu interconnection layers (25,26) are formed on the CF films through an adherence layer (29) comprising a Ti layer and a TiC layer.

USE - Semiconductor device manufacture.

ADVANTAGE - Cu atoms in the interconnection layers do not diffuse into the insulating films because the insulating films are constituted of CF films. The dielectric constants of the CF films are smaller than that of a BCB film.

DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of the device structure.

Insulating films 21-24

Cu interconnection layers 25,26

Ti adherence layer 29

CHOSEN-DRAWING: Dwg.1a/17

TITLE-TERMS:
NON DIFFUSION COPPER INTERCONNECT STRUCTURE SEMICONDUCTOR DEVICE

DERWENT-CLASS: L03 U11

CPI-CODES: L04-C12; L04-C13B;

EPI-CODES: U11-C05D1;

SECONDARY-ACC-NO:
CPI Secondary Accession Numbers: C2000-005920
Non-CPI Secondary Accession Numbers: N2000-017574